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In the Claims:

This listing of claims replaces all prior versions and listing of claims in the application.

1. (Previously presented) A microprocessor comprising:

a processing unit;

a memory comprising a lower memory area and an extended memory area;

an address bus connecting said processing unit to said memory, and comprising a lower address bus for accessing said lower memory area, and an extended address bus for accessing said extended memory area;

means for executing instructions of an instruction set executable by said microprocessor, the instruction set comprising instructions for accessing said memory, a first instruction group comprising instructions for accessing said lower memory area, and a second instruction group distinct from the first instruction group and only comprising all the instructions for accessing said extended memory area; and

means for forcing to zero an extended address transmitted by said extended address bus when executing an instruction in the first instruction group so that said lower memory area is accessed.

2. (Previously presented) A microprocessor according to Claim 1, wherein each location in said memory is associated with a respective access address; the microprocessor further